## REMARKS

### Drawings

The Examiner states, "There is no bitline region 174 in figures 21A, 21B". Figs. 21A, 21B show an integrated circuit before formation of bitline regions 174. The specification is amended to refer to Fig. 30A as showing the bitline regions.

The Examiner states, "There is also no description of layer 230 in figures 16-17". Layer 230 is described in paragraph 0033 (on page 6).

### Claims

1. Claims 22, 29, 30, 33 were objected to. These claims are amended as suggested by the Examiner.

2. Claims 22-42 were rejected under 35 U.S.C. 102(b) as anticipated by Ogura et al., U.S. patent no. 6,388,293 B1.

Claim 22 recites a floating gate. The Examiner states:

> Ogura (see figures 1, 35, 14 ...) teaches ... a floating gate 140 ...

Ogura's gate 140 is not a floating gate. The difference between floating gate memories and Ogura's "carrier trapping" devices is explained in William D. Brown et al., *Nonvolatile Semiconductor Memory Technology* (IEEE Press 1998), pages 5-6 (see Exhibit A attached hereto) as follows:

> The storage of charges in the gate insulator of a MOSFET can be realized in two ways, which has led to the subdivision of nonvolatile semiconductor memory devices into two main classes.
>
> The first class of devices is based on the storage of charge on a conducting or semiconducting layer that is completely surrounded by a dielectric ... Since this layer acts as a completely electrically isolated gate, this type of device is commonly referred to as a floating gate device ...

> In the second class of devices, the charge is stored in discrete trapping centers of an appropriate **dielectric** layer. These devices are, therefore, usually referred to as charge-trapping devices.

Ogura does not teach or suggest that his gate 140 is "completely surrounded by dielectric" as required for a floating gate. Of note, Ogura's memories of Figs. 1, 35, 14 store the charge on a gate insulator 132 (for Figs. 1, 35) or gate insulator 135R (for Fig. 14). See column 6, lines 35-36 and 57-61; column 9, line 66 through column 10, line 1; column 17, lines 63-64 ("gate insulator (132R) with charge storing means"); column 18, lines 18-21. These memories are thus charge-trapping devices which do not need a floating gate.

Claims 23-32 depend from Claim 22.

Claim 33 also recites a floating gate.

Claims 34-42 depend from Claim 33.

3. Claims 22-42 were rejected under 35 U.S.C. 102(b) as anticipated by Harari et al., U.S. patent no. 6,420,231 B1.

Claim 22 recites a "first conductive gate comprising a semiconductor material of a second conductivity type" opposite to the source/drain regions' conductivity type. For example, in Applicant's Fig. 30A, source/drain regions 174 are type N and select gate 140 is type P. In other embodiments, the source/drain regions are type P and the select gate is type N.

It is well known that at least in the PMOS transistor, having the opposite conductivity types may increases the transistor current but undesirably make the transistor "more susceptible to the short channel effects" (specification, page 2, paragraph 0011). The inventor has observed however that at least some nonvolatile memories have longer channels because their channels are formed by "merging together the channel of the floating gate transistor and the channel of the select transistor" (page 2, paragraph 0012). For example, in Fig. 30A, the cell's channel region includes a portion under the select gate 140 and another portion under each floating gate ("FG") 160 that are merged together. Therefore the short channel effects are less of a problem, and the opposite conductivity types become

"an attractive way to increase the transistor current" and hence to speed up the memory. Specification, page 2, paragraphs 0010 and 0012.

Claim 22 is not limited to the embodiments and advantages discussed herein.

The Examiner states:

> Harari (see figures 4, 5 and col. 8, lines 1-39) teaches ... source/drain regions 49, 51 of a first conductivity type ... a first conductive gate 55-58 comprising a semiconductor material of a second conductivity type opposite to the first conductivity type ...

Harari does not teach or suggest that the gates 55-58 have the opposite conductivity type to the source/drain regions 49, 51. The Examiner cites Harari's column 8, lines 1-39, which include the following statement:

> Although use of n-channel semiconductor transistors is preferred, implementation of the present invention is not limited to use of such devices.

This statement, as well as the rest of column 8, lines 1-39 do not indicate whether or not Harari's gates 55-58 are the same or opposite conductivity type as the source/drain regions.

Claim 23 further recites that the first conductive gate is a gate of a "buried channel transistor", i.e. a transistor with "more current flowing below the channel surface than at the channel surface" (specification, page 2, lines 18-20).

Harari does not teach or suggest that his memory has more current flowing below the channel surface as recited in Claim 23.

Claims 24-32 depend from Claim 22.

Claim 33 recites a buried channel transistor (see the discussion of Claim 23).

Any questions regarding this case can be addressed to the undersigned at the telephone number below.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 24, 2005.

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